Amendments to the Claims:

Listing of Claims:

1. (currently amended) A method for dynamically adjusting an operating speed of a microprocessor for the microprocessor to access at least a serial flash memory, wherein the serial flash memory is a program memory, and the digital data stored in the serial flash memory is programming data, the method comprising:

~~(a) reducing an executing speed of the microprocessor if the data that microprocessor required from the serial flash memory is not well prepared; and~~

~~(b) executing the microprocessor at a normal speed if the data that microprocessor required from the serial flash memory is well prepared.~~

(a) providing a buffering/controlling device;

(b) utilizing the buffering/controlling device to access a predetermined number of digital data stored in the serial flash memory;

(c) utilizing the microprocessor to access desired digital data from the buffering/controlling device;

(d) in step (c), utilizing the microprocessor to access the digital data located in the buffering/controlling device and continuing to operate the microprocessor at the normal speed when the desired digital data of the microprocessor are in the buffering/controlling device;

(e) in step (c), reducing the operating speed of the microprocessor when the desired digital data of the microprocessor are not in the buffering/controlling device; and

(f) after proceeding with step (e), transmitting the desired digital data of the microprocessor from the serial flash memory to the buffering/controlling

device and then recovering the operating speed of the microprocessor so that the microprocessor is capable of accessing the digital data.

2. (currently amended) The method of claim 1, wherein in step [[(a)]] (e), reducing the executing speed of the microprocessor makes the executing speed of the microprocessor lower than the normal speed or totally suspends the microprocessor.

3. (currently amended) The method of claim 1, wherein step [[(a)]] (e) is capable of being achieved by adjusting an operating clock with an external circuit or with a circuit installed in the microprocessor[[,]] ; achieved by inserting an NOP (No Operation) command among commands[[,]] ; or achieved by keeping a program counter unchanged.

4. (currently amended) The method of claim 1 ~~involved with a buffering/controlling device~~, wherein transmitting the desired digital data of the microprocessor from the serial flash memory to the buffering/controlling device ~~the method~~ further ~~comprising~~ comprises:

~~(c) utilizing the buffering/controlling device to access a predetermined number of digital data stored in the serial flash memory;~~

~~(d) utilizing the microprocessor to access desired digital data from the buffering/controlling device;~~

~~(e) in step (b), utilizing the microprocessor to access the digital data located in the buffering/controlling device and continuing to operate the microprocessor at the normal speed when the desired digital data of the microprocessor are in the buffering/controlling device;~~

~~(f) in step (a), reducing the operating speed of the microprocessor when the desired digital data of the microprocessor are not in the buffering/controlling device; and~~

~~(g)after proceeding with step (f),~~ transmitting the desired digital data of the microprocessor from the serial flash memory ~~to the buffering/controlling device and~~ to the microprocessor ~~and recovering the operating speed of the microprocessor so that the microprocessor is capable of accessing the digital data~~.

5. (currently amended) The method of claim [[4]] 1 further comprising:

[[(h)]] (g) in step [[(c)]] (b), utilizing the buffering/controlling device to consecutively access the predetermined number of digital data at a starting address of the serial flash memory; and

[[(i)]] (h) in step ~~(d), (e), and (f)~~ (c), (d), and (e), utilizing the microprocessor to emit an access address corresponding to the digital data to the buffering/controlling device, so that the buffering/controlling device is capable of judging whether the desired digital data of the microprocessor are located in the buffering/controlling device.

6. (currently amended) The method of claim [[4]] 1, wherein a first data access rate is set between the buffering/controlling device and the microprocessor, and a second data access rate is set between the memory and the buffering/controlling device, wherein the first data access rate is higher than or equal to the second data access rate.

7. (currently amended) The method of claim [[4]] 1, wherein the buffering/controlling device [[is]] comprises a FIFO storage structure, a dynamic random access memory (DRAM), or a static random access memory (SRAM).

8. (currently amended) A method for dynamically adjusting an operating speed of a microprocessor for the microprocessor to access at least a serial flash memory

and a random access memory (RAM), wherein the serial flash memory and the random access memory are program memories, and the digital data stored in the serial flash memory or the random access memory is programming data, the method comprising:

(a) loading partial of the program codes from the serial flash memory to the random access memory before the microprocessor's requiring data; [[and]]

~~(b)reducing an executing speed of the microprocessor if the data that microprocessor required from the serial flash memory or the random access memory is not well prepared; and~~

~~(c)executing the microprocessor at a normal speed if the data that microprocessor required from the serial flash memory or the random access memory is well prepared.~~

(b) providing a buffering/controlling device;

(c) utilizing the buffering/controlling device to access a predetermined number of digital data stored in the serial flash memory or the random access memory;

(d) utilizing the microprocessor to access desired digital data from the buffering/controlling device;

(e) in step (d), utilizing the microprocessor to access the digital data located in the buffering/controlling device and continuing to operate the microprocessor at the normal speed when the desired digital data of the microprocessor are in the buffering/controlling device;

(f) in step (d), reducing the operating speed of the microprocessor when the desired digital data of the microprocessor are not in the buffering/controlling device; and

(g) after proceeding with step (f), transmitting the desired digital data of the microprocessor from the serial flash memory or the random access memory to the buffering/controlling device and then recovering the operating speed of the microprocessor so that the microprocessor is capable of accessing the digital data.

9. (currently amended) The method of claim 8, wherein in step [[(b)]] (f), reducing the executing speed of the microprocessor makes the executing speed of the microprocessor lower than the normal speed or totally suspends the microprocessor.

10. (currently amended) The method of claim 8, wherein step [[(b)]] (f) is capable of being achieved by adjusting an operating clock with an external circuit or with a circuit installed in the microprocessor[[,]] ; achieved by inserting an NOP (No Operation) command among commands[[,]] ; or achieved by keeping a program counter unchanged.

11. (currently amended) The method of claim 8 ~~involved with a buffering/controlling device~~, wherein ~~the method~~ transmitting the desired digital data of the microprocessor from the serial flash memory or the random access memory to the buffering/controlling device further ~~comprising~~ comprises:

~~(d) utilizing the buffering/controlling device to access a predetermined number of digital data stored in the serial flash memory or the random access memory;~~

~~(e) utilizing the microprocessor to access desired digital data from the buffering/controlling device;~~

~~(f) in step (e), utilizing the microprocessor to access the digital data located in the buffering/controlling device and continuing to operate the microprocessor at the normal speed when the desired digital data of the microprocessor are in the buffering/controlling device;~~

~~(g) in step (b), reducing the operating speed of the microprocessor when the desired digital data of the microprocessor are not in the buffering/controlling device; and~~

~~(h)after proceeding with step (g),~~ transmitting the desired digital data of the microprocessor from the serial flash memory or the random access memory ~~to the buffering/controlling device and~~ to the microprocessor ~~and recovering~~

~~the operating speed of the microprocessor so that the microprocessor is capable of accessing the digital data~~.

12. (currently amended) The method of claim [[11]] 8 further comprising:

[[(i)]] (g) in step [[(d)]] (c), utilizing the buffering/controlling device to consecutively access the predetermined number of digital data at a starting address of the serial flash memory or the random access memory; and

[[(j)]] (h) in step ~~(e), (f), and (g)~~ (d), (e), and (f), utilizing the microprocessor to emit an access address corresponding to the digital data to the buffering/controlling device, so that the buffering/controlling device is capable of judging whether the desired digital data of the microprocessor are located in the buffering/controlling device.

13. (currently amended) The method of claim [[11]] 8, wherein a first data access rate is set between the buffering/controlling device and the microprocessor, and a second data access rate is set between the serial flash memory and the buffering/controlling device, and a third data access rate is set between the random access memory and the buffering/controlling device, wherein the first data access rate is higher than or equal to the second data access rate, and the first data access rate is higher than or equal to the third data access rate.

14. (currently amended) The method of claim [[11]] 8, wherein the buffering/controlling device [[is]] comprises a FIFO storage structure, a dynamic random access memory (DRAM), or a static random access memory (SRAM).

15. (original) The method of claim 8, wherein the random access memory is a dynamic random access memory (DRAM).

16. (currently amended) A method for dynamically adjusting an operating speed of a microprocessor for the microprocessor to access at least a random access memory (RAM), wherein the random access memory are a program memory, and the digital data stored in the random access memory is programming data, the method comprising:

(a)loading the digital data from a serial flash memory to the random access memory before the microprocessor's requiring data; [[and]]

~~(b)reducing an executing speed of the microprocessor if the data that microprocessor required from the random access memory is not well prepared; and~~

~~(c)executing the microprocessor at a normal speed if the data that microprocessor required from the random access memory is well prepared.~~

(b) providing a buffering/controlling device;

(c) utilizing the buffering/controlling device to access a predetermined number of digital data stored in the random access memory;

(d) utilizing the microprocessor to access desired digital data from the buffering/controlling device;

(e) in step (d), utilizing the microprocessor to access the digital data located in the buffering/controlling device and continuing to operate the microprocessor at the normal speed when the desired digital data of the microprocessor are in the buffering/controlling device;

(f) in step (d), reducing the operating speed of the microprocessor when the desired digital data of the microprocessor are not in the buffering/controlling device; and

(g) after proceeding with step (f), transmitting the desired digital data of the microprocessor from the random access memory to the buffering/controlling device and then recovering the operating speed of the microprocessor so that the microprocessor is capable of accessing the digital data.

17. (currently amended) The method of claim 16, wherein in step [[(b)]] (f), reducing the executing speed of the microprocessor makes the executing speed of the microprocessor lower than the normal speed or totally suspends the microprocessor.

18. (currently amended) The method of claim 16, wherein step [[(b)]] (f) is capable of being achieved by adjusting an operating clock with an external circuit or with a circuit installed in the microprocessor[[,]] ; achieved by inserting an NOP (No Operation) command among commands[[,]] ; or achieved by keeping a program counter unchanged.

19. (currently amended) The method of claim 16, ~~involved with a buffering/controlling device, the method~~ wherein transmitting the desired digital data of the microprocessor from the random access memory to the buffering/controlling device further ~~comprising~~ comprises:

~~(d) utilizing the buffering/controlling device to access a predetermined number of digital data stored in the random access memory;~~

~~(e) utilizing the microprocessor to access desired digital data from the buffering/controlling device;~~

~~(f) in step (e), utilizing the microprocessor to access the digital data located in the buffering/controlling device and continuing to operate the microprocessor at the normal speed when the desired digital data of the microprocessor are in the buffering/controlling device;~~

~~(g) in step (b), reducing the operating speed of the microprocessor when the desired digital data of the microprocessor are not in the buffering/controlling device; and~~

~~(h)after proceeding with step (g),~~ transmitting the desired digital data of the microprocessor from the random access memory ~~to the buffering/controlling~~

~~device and~~ to the microprocessor ~~and recovering the operating speed of the microprocessor so that the microprocessor is capable of accessing the digital data~~.

20. (currently amended) The method of claim [[19]] 16 further comprising:

[[(i)]] (h) in step [[(d)]] (c), utilizing the buffering/controlling device to consecutively access the predetermined number of digital data at a starting address of the random access memory; and

[[(j)]] (i) in step ~~(e), (f), and (g)~~ (d), (e), and (f), utilizing the microprocessor to emit an access address corresponding to the digital data to the buffering/controlling device, so that the buffering/controlling device is capable of judging whether the desired digital data of the microprocessor are located in the buffering/controlling device.

21. (currently amended) The method of claim [[19]] 16, wherein a first data access rate is set between the buffering/controlling device and the microprocessor, and a second data access rate is set between the random access memory and the buffering/controlling device, wherein the first data access rate is higher than or equal to the second data access rate.

22. (currently amended) The method of claim [[19]] 16, wherein the buffering/controlling device [[is]] comprises a FIFO storage structure, a dynamic random access memory (DRAM), or a static random access memory (SRAM).

23. (original) The method of claim 16, wherein the random access memory is a dynamic random access memory (DRAM).

24. (original) A method for dynamically adjusting an operating speed of a

microprocessor emulator for the microprocessor emulator to emulate the operation with a serial flash memory, the method comprising:

(a) reducing an executing speed of the microprocessor emulator for a certain period; and

(b) executing the microprocessor emulator at a normal speed after the certain period.

25. (original) The method of claim 24, wherein in step (a) and (b), the certain period depends on the serial flash access time.

26. (original) The method of claim 24, wherein in step (a), reducing the executing speed of the microprocessor emulator makes the executing speed of the microprocessor emulator lower than the normal speed or totally suspends the microprocessor emulator.

27. (original) The method of claim 24, wherein step (a) is capable of being achieved by adjusting an operating clock with an external circuit or with a circuit installed in the microprocessor emulator[[,]] ; achieved by inserting an NOP (No Operation) command among commands[[,]] ; or achieved by keeping a program counter unchanged.

28. (original) The method of claim 24, wherein the microprocessor emulator is electrically connected to a microprocessor system that further comprises a buffering/controlling device, the method comprising:

(c) utilizing the microprocessor emulator to emit an access address to the buffering/controlling device;

(d) in step (b), operating the microprocessor emulator at the normal speed when the access address is in the buffering/controlling device; and

(e) in step (a), reducing the operating speed of the microprocessor emulator when the access address is not in the buffering/controlling device.

29. (original) The method of claim 28 further comprising:

(f) after proceeding with step (e), recovering the operating speed of the microprocessor emulator after a predetermined number of clock cycles.

30. (original) The method of claim 24, wherein the microprocessor emulator is electrically connected to a second memory, and the second memory is capable of being used to transmit at least an instruction to the microprocessor emulator.

31. (original) The method of claim 30, wherein the second memory is a static random access memory (SRAM), a flash memory, or a dynamic random access memory (DRAM).

32. (currently amended) The method of claim 28, wherein the buffering/controlling device is electrically connected to the serial flash memory, and the serial flash memory stores a plurality of digital data, the method further comprising:

(g) utilizing the buffering/controlling device to access a predetermined number of digital data stored in the serial flash memory;

(h) in step (d), utilizing the buffering/controlling device to transmit the digital data corresponding to the access address to the microprocessor emulator when the access address is in the buffering/controlling device; and

(i) after proceeding with step (e), transmitting the digital data corresponding to the access address from the serial flash memory to the buffering/controlling device and ~~to the microprocessor emulator and~~ then recovering the executing speed of the microprocessor emulator.

33. (original) The method of claim 32, wherein in step (g), the buffering/controlling device consecutively accesses the predetermined number of digital data at a starting address of the serial flash memory.

34. (original) The method of claim 32, wherein the serial flash memory is a program memory, and the digital data stored in the serial flash memory are programming codes.

35. (original) The method of claim 32, wherein a first data access rate is set between the buffering/controlling device and the microprocessor emulator, and a second data access rate is set between the serial flash memory and the buffering/controlling device, wherein the first data access rate is higher than or equal to the second data access rate.

36. (original) The method of claim 24, wherein the operating clock's frequency of the microprocessor emulator is capable of being adjusted by an external clock device.

37. (currently amended) The method of claim 28, wherein the buffering/controlling device [[is]] comprises a FIFO storage structure, a dynamic random access memory (DRAM), or a static random access memory (SRAM).

38. (original) The method of claim 24, wherein the microprocessor emulator is an in-circuit emulator.

39. (new) The method of claim 32, wherein transmitting the digital data corresponding to the access address from the serial flash memory to the buffering/controlling device further comprises transmitting the digital data corresponding to the access address from the serial flash memory to the microprocessor emulator.